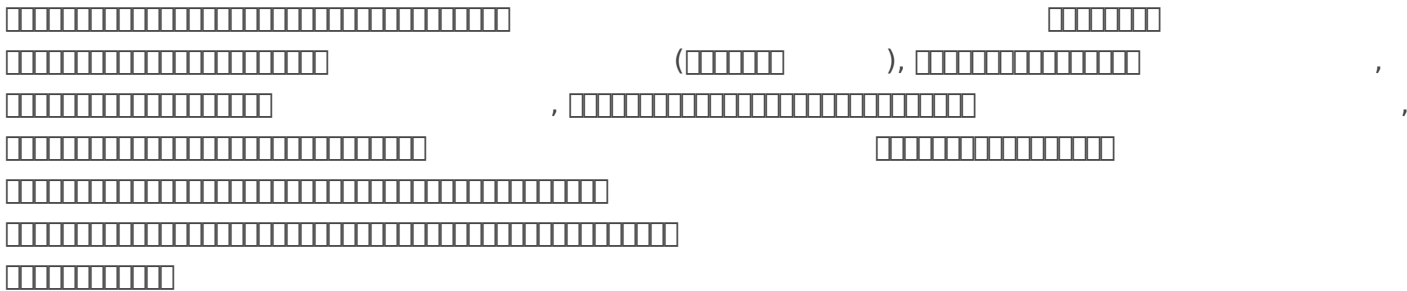


Diagram illustrating the memory layout for a 100-bit instruction. The layout is divided into six rows, each representing a different instruction format or state. The total width of the diagram is 100 bits.

- Row 1: 10 bits of instruction, 10 bits of ISEO, 10 bits of IsOn.
- Row 2: 100 bits of instruction.
- Row 3: 10 bits of instruction, 10 bits of instruction, 10 bits of instruction.
- Row 4: 10 bits of instruction, 10 bits of CEO, 10 bits of instruction, 10 bits of instruction, 10 bits of instruction.
- Row 5: 100 bits of instruction.
- Row 6: 10 bits of instruction.



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Revision #2

Created 17 August 2023 01:51:28 by CAT3 [REDACTED]

Updated 30 August 2023 07:39:26 by CAT3 [REDACTED]

[REDACTED] ([REDACTED])

[REDACTED] ([REDACTED])