

WI-WH-010

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4.

The diagram illustrates a 16-bit bus architecture. At the top, a horizontal bar represents the bus, with a label '16-bit bus' and a 'GR' (General Register) connected to it. Below the bus, several components are shown:

- Memory Banks:** Two banks of memory are shown, each consisting of 16 small squares representing 16-bit words. The left bank is labeled 'Memory Bank 1' and the right bank is labeled 'Memory Bank 2'.
- Control Signals:** A series of control signals are shown below the memory banks, including 'Chip Select', 'Read/Write', and 'Clock'.
- Address and Data Buses:** The diagram shows the flow of data and addresses between the CPU and memory. The address bus is labeled 'Address Bus' and the data bus is labeled 'Data Bus'.

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5. XXXXXXXXXX

5.1. XXXXXXXXXX

5.1.1. XXXXXXXXXX

5.1.2. XXXXXXXXXX

5.1.3. XXXXXXXXXX Supplier

5.2. XXXXXXXXXXXXXXXXXXXX /XXXXXXX

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5.2.1. XXXXXXX XXXXXXX Pass XXX

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5.2.2.1. XXXXXXXXXXXXXXX

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5.2.2.2. LP GR

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5.2.4.

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5.3.







[illegible]

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5.4. GR  
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5.4.1. 





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5.4.2. GR   GR 
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5.4.3. 

 GR 

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5.5.4.

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Revision #4

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